IN THE CLAIMS:

Please amend claims 1-4, 7, 9-12, 15, 17-25, and 29 as follows:

1. (Currently Amended) A receiver comprising:

an input in the receiver which receives a time division multiplexed signal containing a plurality of channels which has been transmitted from a transmitter;

a memory coupled to the input, including an addressable storage array which stores a sequence of data samples contained in the time division multiplexed signal from the plurality of channels with each successive data sample belonging to a channel different than a channel to which an immediately preceding data sample belongs and outputs the stored data samples in a sequence of data groups equal in number to a number of the plurality of channels with each data group containing a plurality of samples from one of the plurality of channels; and

a decoder, responsive to the sequence of data groups, which decodes the data samples within the sequence of data groups and outputs decoded data samples of the plurality of data groups from the plurality of channels.

2. (Currently Amended) A receiver in accordance with claim 1 comprising:

a multichannel phase tracking which processes the data groups from the plurality of channels to output from each data group a group of most likely bits; and wherein

the data samples each comprise orthogonally encoded data; and

the decoder is a biorthogonal inner code soft decision data decoder which decodes groups of most likely bits.

3. (Currently Amended) A receiver in accordance with claim 30 wherein:

the biorthogonal inner code soft decision data decoder is a Reed-Muller decoder.

4. (Currently Amended) A receiver in accordance with claim 3 wherein:

the orthogonally encoded data samples are QPSK encoded.

5. (Original) A receiver in accordance with claim 1 wherein:

the receiver is contained in a satellite.

6. (Original) A receiver in accordance with claim 2 wherein:

the receiver is contained in a satellite.

7. (Currently Amended) A receiver in accordance with claim 30 wherein:

the receiver is contained in a satellite.

8. (Original) A receiver in accordance with claim 3 wherein:

the receiver is contained in a satellite.

9. (Currently Amended) A receiver in accordance with claim 5 further comprising:

a channelizer coupled to the input and to the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

10. (Currently Amended) A receiver in accordance with claim 6 further comprising:

a channelizer coupled to the input and to the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

11. (Currently Amended) A receiver in accordance with claim 7 further comprising:

a channelizer coupled to the input and to the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

12. (Currently Amended) A receiver in accordance with claim 8 further comprising:

a channelizer coupled to the input and the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

13. (Original) A receiver in accordance with claim 1 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

14. (Original) A receiver in accordance with claim 2 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

15. (Currently Amended) A receiver in accordance with claim 30 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

16. (Original) A receiver in accordance with claim 5 wherein:

each of the at least one memory further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write

address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the write address generator and the sequence of data groups being read out with addresses generated by the read address generator;

the another memory further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells of the another memory with addresses generated by the write address generator and the sequence of data groups being read out from a group of memory cells of the another memory with addresses generated by the read address generator.

17. (Currently Amended) A method of data reception comprising:

in a receiver receiving and storing a time division multiplexed signal transmitted from a transmitter containing a sequence of data samples from a plurality of channels with each successive data sample belonging to a channel different than a channel to which an immediately preceding data sample belongs;

outputting the stored data samples in a sequence of data groups equal in number to a number of the plurality of channels, each data group containing a plurality of samples from one of the plurality of channels;

decoding the data samples within the sequence of data groups; and

outputting the decoded data samples of the plurality of data groups from the plurality of channels .

18. (Currently Amended) A method in accordance with claim 17 wherein:

performing multiphase tracking of the data groups from the plurality of channels to output from each group a group of most likely bits; and wherein

the data samples each comprise orthogonally encoded data; and

the decoder is an inner code soft decision biorthogonal decoder which decodes groups of most likely bits.

19. (Currently Amended) A method in accordance with claim 32 wherein:

the orthogonally encoded data samples are QPSK encoded.

20. (Currently Amended) A method in accordance with claim 17 wherein:

the receiver is contained in a satellite.

21. (Currently Amended) A method in accordance with claim 18 wherein:

the receiver is contained in a satellite.

22. (Currently Amended) A method in accordance with claim 32 wherein:

the receiver is contained in a satellite.

23. (Currently Amended) A method in accordance with claim 20 wherein:

an input bandwidth from the transmitter is received by the receiver and is divided by the receiver with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

24. (Currently Amended) A method in accordance with claim 21 wherein:

an input bandwidth from the transmitter is received by the receiver and is divided by the receiver with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

25. (Currently Amended) A method in accordance with claim 22 wherein:

an input bandwidth from the transmitter is received by the receiver and is divided by the receiver with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

26. (Original) A method in accordance with claim 20 further comprising:

addressing memory cells of each of the at least one memory by addresses generated by a read address generator and a write address generator, the sequence of data samples being written in a data group of memory cells by addresses generated by the write address generator and the

sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

27. (Original) A method in accordance with claim 21 further comprising:

addressing memory cells of each of the memories and the another memory by addresses generated by write address generators and read address generators, the sequence of data samples being written in a group of memory cells by addresses generated by the write address generators and the sequence of data groups outputted from the memories and the another memory being generated by addresses generated by the read address generators.

28. (Original) A method in accordance with claim 22 further comprising:

addressing memory cells of each of the at least one memory by addresses generated by a read address generator and a write address generator, the sequence of data samples being written in a data group of memory cells by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

29. (Currently Amended) A method in accordance with claim 32 wherein:

the data samples are stored in an addressable storage array containing memory cells which are addressed by a pair of addresses, the sequence of data samples being written in a group of memory cells each containing one common address of the pair of addresses and the sequence of data groups are each individually outputted from a group of memory cells containing one common address which is another of the pair of addresses.

Please insert new claims 30-35 as follows:

30. (New) A receiver in accordance with claim 2 comprising:

an outer decoder, coupled to the inner decoder, which sequentially decodes blocks of data including the most likely bits from the plurality of channels.

31. (New) A receiver in accordance with claim 30 wherein:

the multichannel phase tracking outputs hard decisions from the multiple channels which are coupled to the outer decoder and the blocks of data include the hard decisions which are also decoded by the outer decoder.

32. (New) A method in accordance with claim 18 comprising:

sequentially decoding blocks of data including the most likely bits from the plurality of channels.

33. (New) A method in accordance with claim 32 wherein:

the multichannel phase tracking outputs hard decisions from multiple channels which are coupled to the outer decoder and the blocks of data include the hard decisions which are also decoded by the outer decoder.

34. (New) A satellite data reception system comprising:

a channelizer which receives a frequency spectrum containing samples of a band transmitted from a transmitter over a wireless link and divides the frequency spectrum into subbands including a sequence of the data samples comprising a time division multiplexed signal from multiple channels output by the channelizer with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs;

a multiple channel phase tracking coupled to the time division multiplexed signal from the multiple channels which outputs sequentially groups of most likely bits and from hard decisions from multiple channels;

a first memory, coupled to groups of most likely bits, which stores the groups of most likely bits from the multiple channels and outputs a sequence

of data groups equal to a number of the multiple channels with each data group containing a plurality of samples from one of the multiple channels;

an inner decoder, responsive to the sequence of data groups from the first memory, which outputs decoded data groups from the multiple channels;

a second memory, coupled to the decoded data groups from the multiple channels and to the hard decisions from multiple channels, which stores the decoded data groups and the hard decisions into data blocks which are sequentially output by the second memory; and

an outer decoder which decodes the sequentially output data blocks from the second memory.

35. (New) A method of receiving data in a satellite which is transmitted from a transmitter over a wireless link that is received with a data receiving system including a channelizer, a multiple channel phase tracker, a first memory, an inner decoder, a second memory and an outer decoder comprising:

receiving with the channelizer a frequency spectrum containing data samples transmitted from the transmitter and dividing the frequency spectrum into subbands, including a sequence of data samples comprising a time division multiplexed signal output from multiple channels with each successive data sample belonging to a channel different from a channel to which an immediate preceding data sample belongs;

the multiple channel phase tracking in response to the time division multiplexed signal from the multiple channels sequentially outputs groups of most likely bits and hard decisions from the multiple channels;

storing with the first memory groups of most likely bits from the multiple channels and outputting a sequence of data groups equal to a number of the multiple channels with each data group containing a plurality of samples from one of the multiple channels;

the inner decoder, in response to the output of data groups from the first memory, outputs decoded data groups from the multiple channels;

the second memory in response to the decoded data groups and to the hard decisions, stores and sequentially outputs the decoded data groups and the hard decisions into data blocks; and

the outer decoder, in response to the sequential output of the stored data blocks from the second memory, sequentially decodes the data blocks.